FEATURES

- Hot-pluggable QSFP-DD
- Compliant with QSFP-DD MSA standard
- Compliant with IEEE 802.3cm 400GBASE-SR8 standard
- Digital diagnostic functions
- 8 channels full-duplex transceiver module
- Supports 425Gb/s aggregate bit rate
- 8 channels 850nm VCSEL array
- 8 channels PIN photo detector array
- Maximum link length of 70m OM3, 100m OM4, 150m OM5
- Single MPO-16 receptacle
- Maximum power dissipation<10W
- Operating case temperature range 0 to 70°C
- Single 3.3V power supply
- RoHS compliant

APPLICATIONS

- Data Center Interconnect
- 400GBASE-SR8 400G Ethernet

DESCRIPTIONS

OPDJ01-8 is a parallel 400Gb/s Quad Small Form Factor Pluggable--double density (QSFP-DD) SR8 optical module designed for optical communication applications. The optical module uses a 4-level pulse am-plitude modulation (PAM4) format. The optical module provides point-to-point 400 Gigabit Ethernet links over eight pairs of multimode fiber, with a reach of up to at least 150m for OM5 (MMF) and 100m for OM4 (MMF) and 70m for OM3 (MMF).
It is compliant with QSFP-DD MSA standard and IEEE 802.3cm 400GBASE-SR8 standard and OIF-CEI-56G-VSR-PAM4 standard. Digital diagnostics functions are available via the I2C interface, as specified by the QSFP-DD MSA.
The QSFP-DD SR8 module edge connector consists of 76 pads.
The pads are designed for a sequenced mating:
First mate – ground pads
Second mate – power pads
Third mate – signal pads
The power supply has six designated pins, VccTx, VccTx1, Vcc1, Vcc2, VccRx, VccRx1 in the connector. Vcc1 and Vcc2 are used to supplement VccTx, VccTx1, VccRx or VccRx1 at the discretion of the module vendor. A single 3.3V Power supply is applied concurrently to these pins.
In addition to the 2-wire serial interface the module has the following low speed signals for control and

status: ModSelL, ResetL, InitMode ,ModPrsL ,IntL.
The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.
InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module. The Init-Mode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transit to High Power Mode after the management interface is initialized.
The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.
IntL is an output signal. The IntL signal is an open collector output and must be pulled up to VccHost on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2 wire serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read.
Low speed signals other than the SCL and SDA interface is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

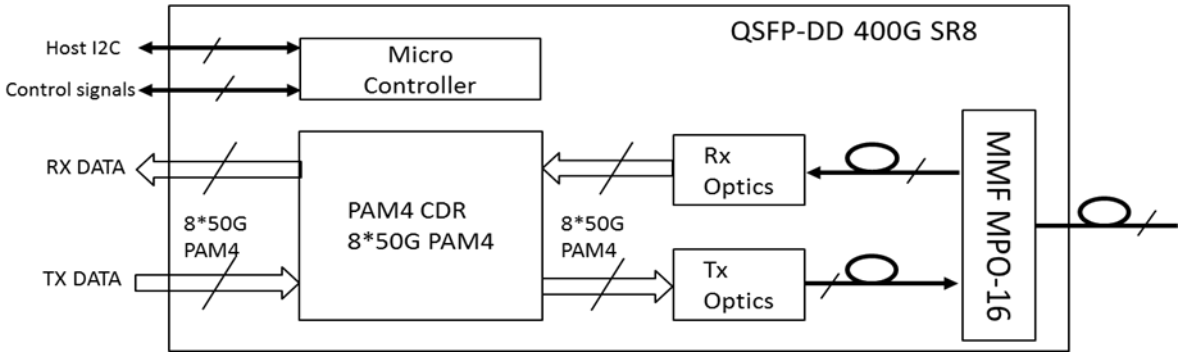

Figure 1. Transceiver Block Diagram

Pin Descriptions

The QSFP-DD SR8 module edge connector consists of a single paddle card with 38 pads on the top and 38 pads on the bottom for a total of 76 pads. The pads are defined in such a manner so as to accommodate insertion of a QSFP module into a QSFP-DD receptacle.

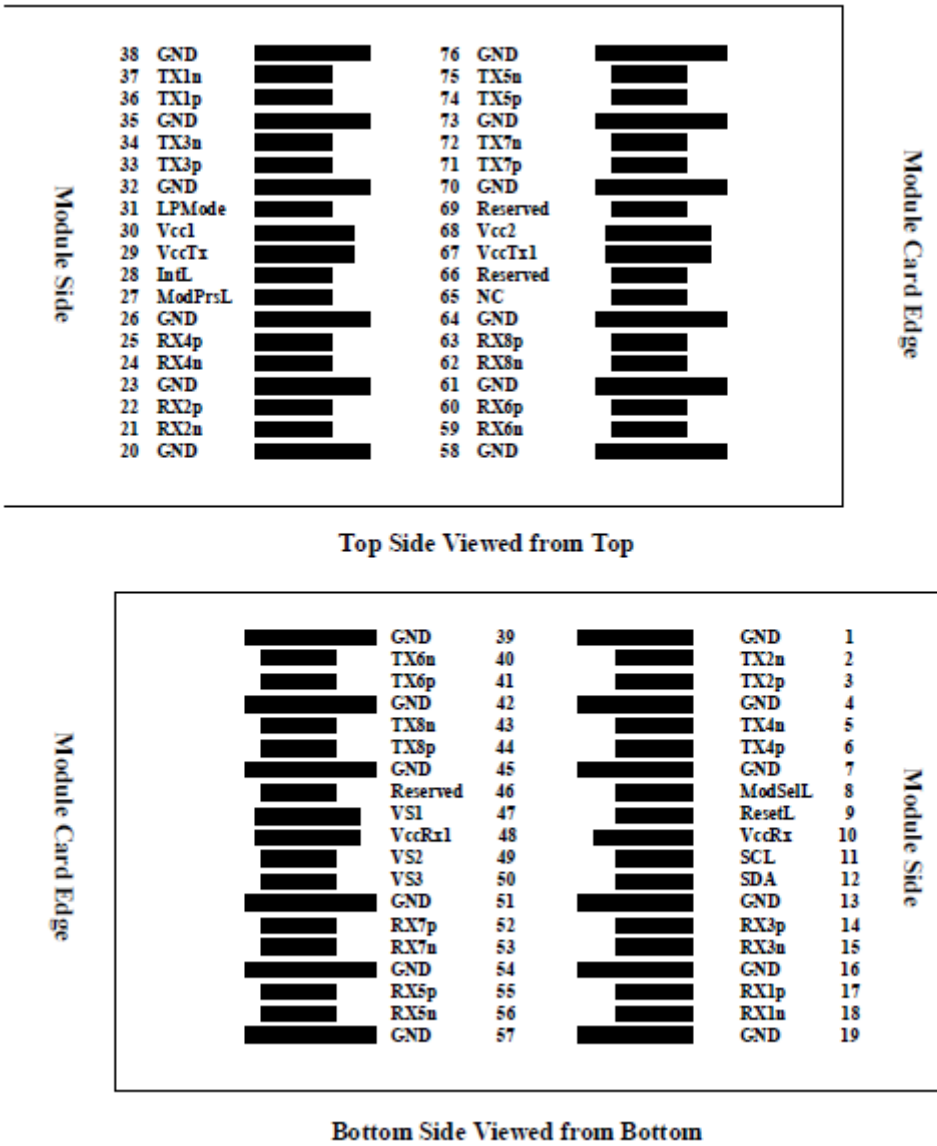

Figure 2. MSA compliant Connector

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1

5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1

46		Reserved	For Future Use	
47		VS1	Module Vendor Specific 1	
48		Vcc Rx1	+3.3V Power Supply Receiver	2
49		VS2	Module Vendor Specific 2	
50		VS3	Module Vendor Specific 3	
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output t	
64		GND	Ground	1
65		NC	For Future Use	
66		Reserved	Interrupt	
67		Vcc Tx1	+3.3V Power supply transmitter	2
68		Vcc2	+3.3V Power supply	2
69		Reserved	For Future Use	
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	GND	1

Notes:

1.QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referred to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2.VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. Each con- nector Vcc pin is rated for a maximum current of 1000 mA.

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause perma- nent damage to this module

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	0	3.3	3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	0		85	%	1
Damage Threshold, each lane	THd	5			dBm	

Notes:

1.Non-condensing

Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless oth-erwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.135	3.3	3.465	V
Case Temperature	Top	0		70	℃
Data Rate, each lane			53.125		Gb/s
Data Rate Accuracy		-100		100	ppm
Link Distance with OM3 MMF				70	m
Link Distance with OM4 MMF				100	m
Link Distance with OM5 MMF				150	m

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power dissipation			9	10	W	Preliminary
Steady state current	Icc	See Note 1			mA	1
Instantaneous peak current				4000	mA	1
Sustained peak current				3300	mA	
Module-to-Host Electrical Specifications at TP4						
Data Rate, each lane			53.125		Gb/s	
Differential Voltage pk-pk	Vpp			900	mV	
Common Mode Voltage	Vcm	-350		2850	mV	
Transition time	Trise/Tfall	9.5			ps	20%~80%
Differential Termination Re- sistance Mismatch				10	%	At 1 MHz
Near-end Eye Width at 10-6 probability (EW6)	EW6	0.265			UI	
Near-end Eye Height at 10-6 probability (EH6)	EH6	70			mV	
Far-end Eye Width at 10-6 probability (EW6)	EW6	0.20			UI	
Far-end Eye Height at 10-6 probability (EH6)	EH6	30			mV	
Near-end Eye Linearity		0.85				
Host-to-Module Electrical Specifications (module input)						
Data Rate, each lane			53.125		Gb/s	
Differential Termination Re- sistance				10	%	At 1 MHz
Overload Differential Voltage pk-pk	Vpp	900		-	mV	TP1a
Common Mode Voltage	Vcm	-350		2850	mV	TP1
Differential Return Loss (SDD11)						TP1
Differential to Common Mode Conversion (SCD11)						TP1

Notes

The module must stay within its declared power class.

Optical Characteristics

Parameter	Min	Typ	Max	Unit	Notes
Transmitter					
Average launch power, each lane	-6.0		4	dBm	
RMS spectral width			0.6	nm	
Extinction ratio, each lane	3			dB	
Line wavelengths	840		860	nm	
Outer Optical Modulation Am- plitude (OMAouter), each lane	-4.5		3	dBm	
Average launch power of OFF transmitter, each lane			-30	dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane			4.5	dB	
TDECQ – 10log10(Ceq)c, each lane			4.5	dB	
Launch power in OMAouter mi- nus TDECQ	-5.9			dBm	
Optical return loss tolerance			12	dB	
Encircled flux	≥86% at 19um ≤30% at 4.5um				
Receiver					
Line wavelengths	840		860	nm	
Average receiver power, each lane	-8.4		4	dBm	
Receiver power, each lane (OMA)			3	dBm	
Damage threshold, each lane	5			dBm	
Receiver sensitivity (OMAouter), each lane			Max(−6.5,SECQ −7.9)	dB	
Pre-FEC bit Error Ratio			2.4e-4		
Stressed receiver Sensitivity (OMA) each lane			-3.5	dBm	

Mechanical Specifications

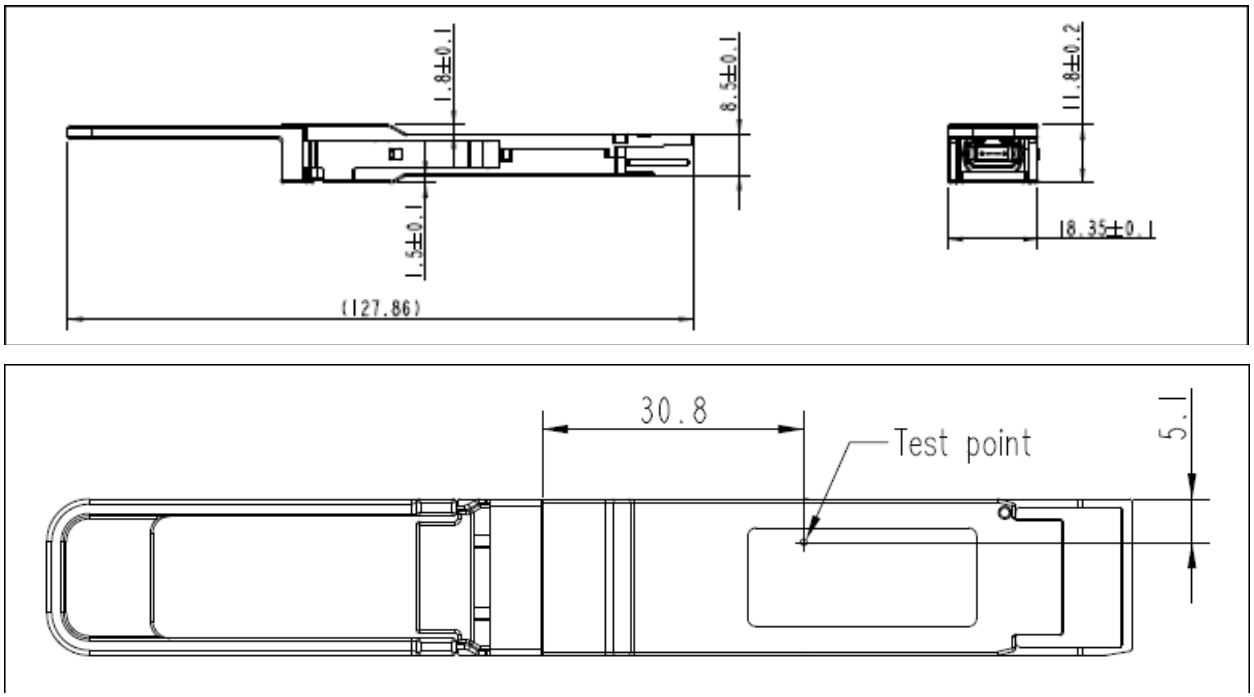

Figure 3. Mechanical Dimensions

In order to ensure the accuracy of the test, it is proposed to use the T 0.08mm type thermocouple as the standard test wire which can be pasted at the shell temperature test point with the glue (recommended Le Tai 416).

Optical Interface

The 400G QSFP-DD SR8 optical interface port shall be either a male MPO receptacle. The recommended lo- cation and numbering of the optical ports for each of the Media Dependent Interfaces is shown in Figure 5. The transmitter and receiver optical lanes shall occupy the positions depicted in Figure 5 when looking into the MDI receptacle with the connector keyway feature on top.

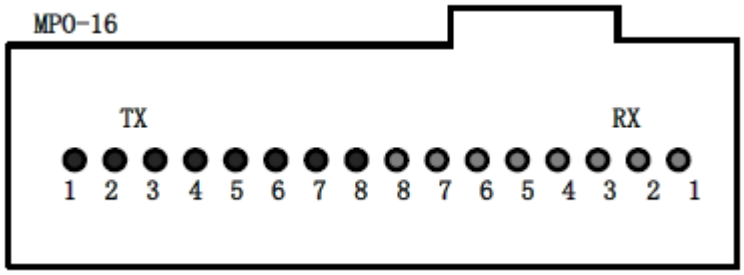

Figure 4. Optical Media Dependent Interface port assignments

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ESD Design

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD pro- tected environment utilizing standard grounded benches, floor mats, and wrist straps.

Parameter	Threshold	Notes
ESD of all the QSFP-DD module pins	1KV	Human Body Model
Air discharge during operation	15KV	
Direct contact discharges to the case	8KV	

Safety Specification Design

Do not look into fiber end faces without eye protection using an optical meter (such as magnifier and micro-scope) within 100 mm, unless you ensure that the laser output is disabled. When operating an optical meter, observe the operation requirements.
CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part No.	Application	Data Rate	Temperature Rating
OPDJ01-8	400GBASE-SR8	400GB Ethernet	0 ~ 70℃

WARNINGS

- Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.
- Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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