FEATURES

- QSFP28 MSA compliant
- Compliant to IEEE 802.3cd Standard
- Hot pluggable 38 pin electrical interface
- 1x50G PAM4 LAN-WDM transmitter
- 26.5625 Gbit/s Channel Electrical Serial Interface (50GAUI-2)
- Maximum power consumption 3.5W
- LC duplex connector
- Supports 53.125Gb/s aggregate bit rate
- Up to 10km transmission on single mode fiber
- Operating case temperature: 0℃ to 70℃
- Single 3.3V power supply
- RoHS compliant

APPLICATIONS

- 50GBASE-LR
- Telecom networking

DESCRIPTIONS

OPQG10 QSFP28 transceiver module is designed for use in 50 Gigabit Ethernet links on up to 10km of single mode fiber. They are compliant with the QSFP28 MSA (SFF-8679 SFF-8636, etc), IEEE P802.3cd. Digital diagnostic functions are available via the I2C interface, as specified by the MSA. A block diagram is shown in Figure 1.

Transceiver Block Diagrams

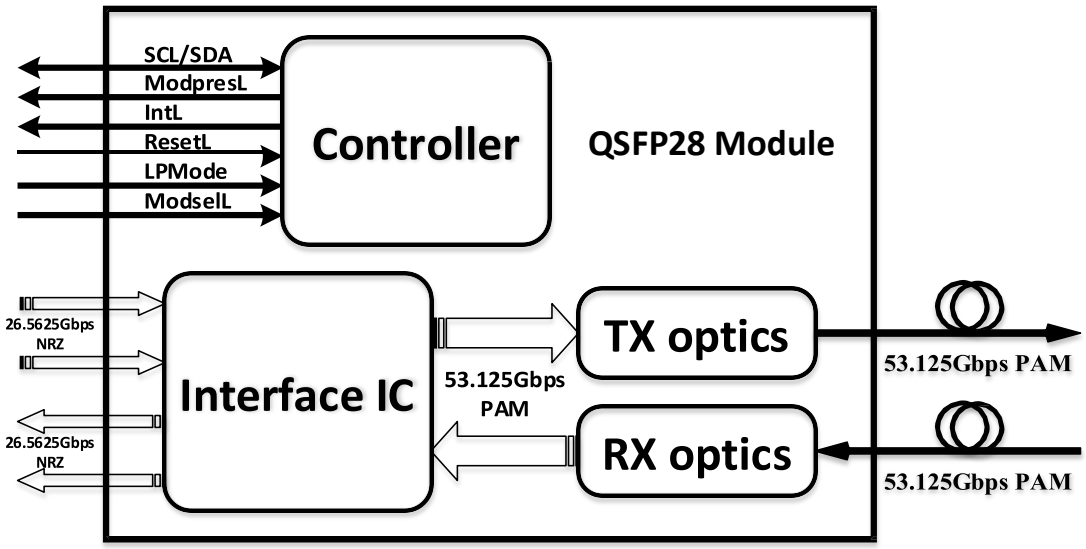

Figure 1. Transceiver Block Diagram

ModSelL:

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL :

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode:

The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2). The host controls how much power a module can consume.

ModPrsL:

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL:

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deas-serted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

Pin Descriptions

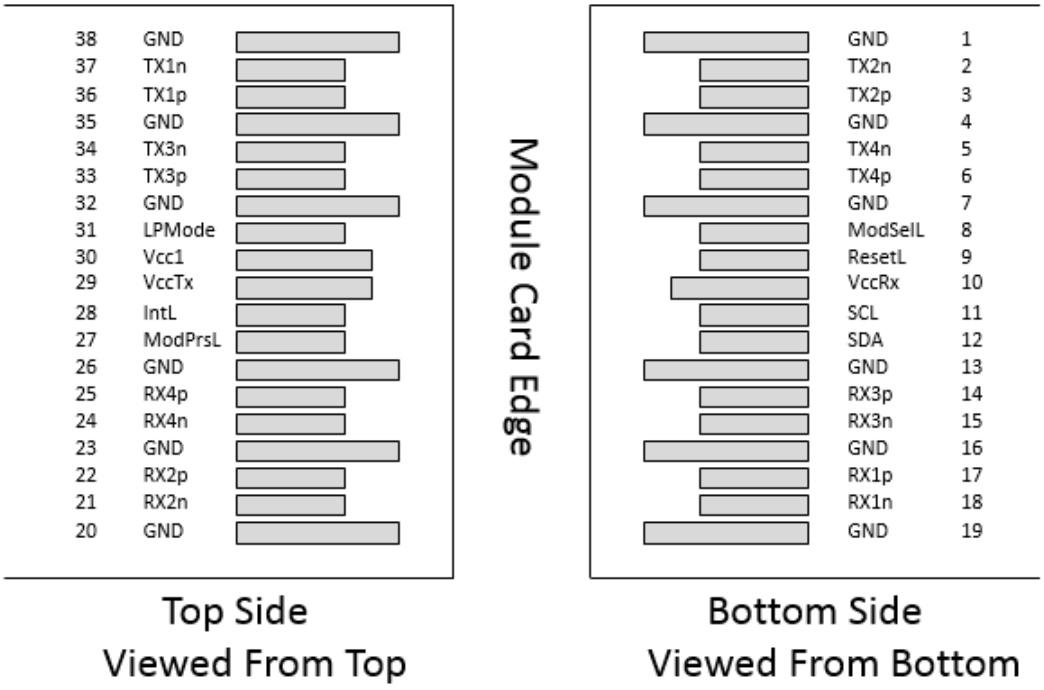

Figure 2. MSA compliant Connector

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Reserved	
6	Tx4p	Reserved	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Reserved	
15	Rx3n	Reserved	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Reserved	
25	Rx4p	Reserved	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Reserved	
34	Tx3n	Reserved	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes

1. Circuit ground is internally isolated from chassis ground.

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	0		3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	10		85	%	1
Damage Threshold	THd	5.2			dBm	

Notes
1. Non-condensing

Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.135	3.3	3.465	V
Case Temperature	Top	0		70	℃
Link Distance with G.652		0.002		10	km

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power dissipation				3.5	W	
Supply Current	Icc			1.0101	A	1
Transmitter						**2**
Data Rate,			26.5625		Gbps	
Differential Voltage pk-pk	Vpp			900	mV	
Common Mode Noise, RMS	Vrms			17.5	mV	
Differential Termination Resistance Mismatch				10	%	At 1 MHz

Transition time	Trise/Tfall	10			ps	20%~80%
Eye width	EW15	0.46			UI	
Eye height	EH15	95			mV	
Receiver						**3**
Data Rate			26.5625		Gbps	
Differential Voltage pk-pk	Vpp			900	mV	
Common Mode Voltage	Vcm	-350		2850	mV	
Common Mode Noise, RMS	Vrms			17.5	mV	
Transition time	Trise/Tfall	9.5			ps	20%~80%
Vertical Eye Closure (VEC)				5.5	dB	
Eye width	EW15	0.57			UI	
Eye height	EH15	228			mV	

Notes:
1, Maximum total power value is specified across the full temperature and voltage range.
2, Refer to OIF-CEI-03.1, CEI-28G-VSR Interface 13.3.2.
3, Refer to OIF-CEI-03.1, CEI-28G-VSR Interface 13.3.3.

Optical Characteristics

50GBASE-LR Operation（EOL, TOP = 0 to +70°C, VCC = 3.135 to 3.465 Volts）

Parameters	Unit	min	type	max	Note
Transmitter					**1**
Signaling Speed	Gb/s	26.5625 ± 100 ppm			
Transmit wavelengths	nm	1304.5		1317.5	
Average Launch Power	dBm	-4.5		4.2	
Outer Optical Modulation Amplitud, (OMAouter)	dBm	-1.5		4	
Launch power in OMAouter minus TDECQ	dBm	-2.9			
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	dB			3.2	
Extinction Ratio (ER)	dB	3.5			
Side-Mode Suppression Ratio (SMSR)	dB	30			

Transmitter reflectance	dB			-26	
Receiver					**1**
Signaling Speed	Gb/s		26.5625 ± 100 ppm		
Receive wavelengths	nm	1304.5		1317.5	
Average receiver power	dBm	-10.8		4.2	
Receiver power (OMAouter)	dBm			4	
Receiver sensitivity	dBm			-8.4	2
Stressed receiver sensitivity (OMAouter)	dBm			-6.6	
LOS Assert	dBm	-30			
LOS Deassert	dBm			-11	
LOS Hysteresis	dB	0.5			
Receiver reflectance	dB			-26	
Conditions of stressed receiver sensitivity test:					
Stressed eye closure for PAM4 (SECQ)	dB		3.2		2
SECQ-10log10(Ceq)	dBm			3.2	2

Notes：

1, Refer to IEEE P802.3cn.

2, RS=max(-8.4, SECQ-9.8) (dBm). For the requirement of receiver sensitivity, the value of BER is 2e-4(before FEC) and within the average receive power, the BER is 1e-12(after FEC).

Mechanical Specifications

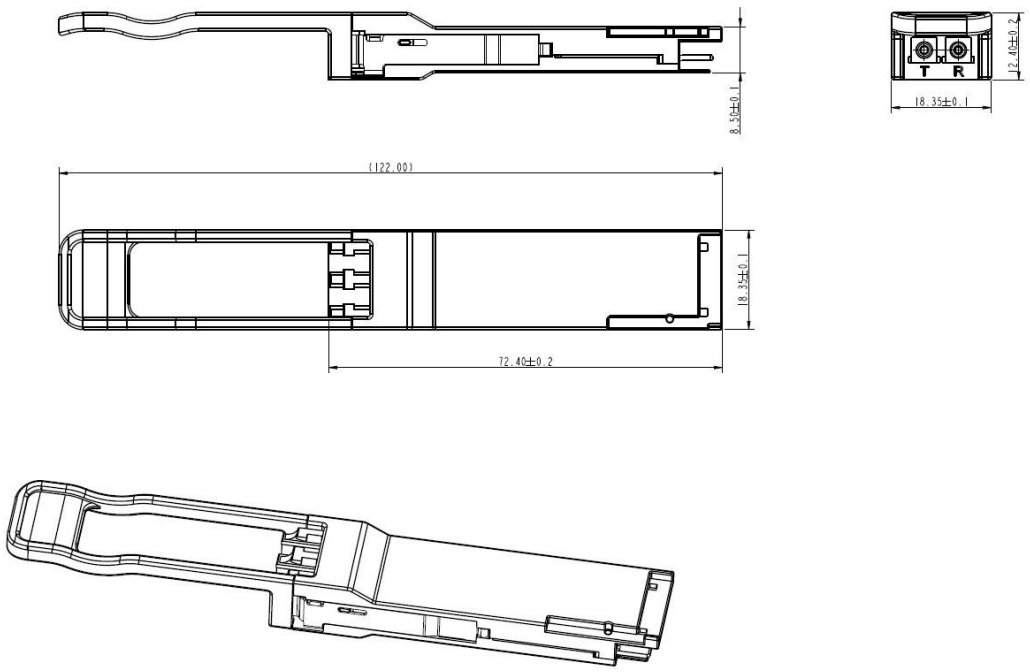

Figure 3. Mechanical Dimension